InGaAs Quantum-Well MOSFET Arrays for Nanometer-Scale Ohmic Contact Characterization

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***Abstract*— We demonstrate InGaAs quantum-well (QW) MOSFET arrays with Mo contact lengths between 40 and 800 nm fabricated by a self-aligned process. A gate pitch of 150 nm is realized, which is the smallest at present for any type of InGaAs FET structure. Fabricated gated MOSFET arrays and gate-less arrays are used to study the properties of nanoscale ohmic contacts in InGaAs MOSFETs with different contact lengths. A three-layer resistive-network model is developed to analyze the contact electrical characteristics. From this paper, we extract a contact resistivity from Mo to n^+ InGaAs of $8 \times 10^{-9}\ \Omega \cdot cm^2$, and from n^+ InGaAs to the QW channel of $2 \times 10^{-8}\ \Omega \cdot cm^2$. When benchmarked with other ohmic contact technologies for n-type InGaAs MOSFETs, our refractory metal contact approach represents the lowest film resistivity and is among the lowest contact resistivity that has been demonstrated. The contact model developed here infers a contact resistance from the Mo contact to the channel of 260 $\Omega \cdot \mu$m for a contact length of $L_c = 10$ nm. This suggests that further research on low-resistance ohmic contacts is required before InGaAs MOSFETs can deliver the required performance.**

***Index Terms*— III–V, contact resistivity, film resistivity, MOSFETs, nanocontacts, self-aligned, tight pitch.**

I. Introduction

InGaAs is a promising candidate as an n-type channel material for future CMOS applications due to its superior electron transport properties [1], [2]. Contacts in CMOS devices must fulfill several stringent requirements. The first one is high-level self-alignment, in which the critical dimensions of the transistor must be defined by single mask level. This is needed in order to achieve a tight device footprint, which includes a gate, a contact, and two spacers. Second, the selection of contact materials and fabrication process should be CMOS-compatible. In addition to the process requirement, the contact technology must also be able to deliver low film resistivity and low contact resistivity. ITRS has set a very challenging goal for high-performance (HP) devices. For 2018, the maximum allowable access resistance is 60 $\Omega \cdot \mu$m (one side) at a contact size of $\sim$10 nm [3]. In light of this demanding goal, contacts to III–V MOSFETs remain a great challenge today.

Contact technology in early n-type InGaAs MOSFETs was inherited from high-electron mobility transistors (HEMTs) [4]. These were based on Au-alloys and fabricated by liftoff [5]–[7]. Some MOSFET prototypes claiming self-aligned architectures actually do not include self-aligned ohmic contacts. The level of self-alignment in those devices is merely up to the heavily doped source and drain (SD), which are made by either implantation [5], [6] or selective epitaxial regrowth [8].

Recently, refractory-metal nonalloyed ohmic contacts on n-type InGaAs HEMTs and MOSFETs have attracted increasing attention due to their low contact resistivity, Si compatibility, and process simplicity [9]–[14]. Nano-Transfer Length Measurement (TLM) [15] and Fin contact structures [16] have been fabricated to study Mo contacts. This refractory metal can be etched by F-based reactive ion etching (RIE) with high selectivity over InGaAs. This allows for a true self-aligned contact with the gate [11]–[13]. RIE damage to the III–V layers can be repaired by thermal annealing at a moderate temperature [17]. Under proper deposition and processing conditions, Mo and other refractory metals, such as W, exhibit very low film resistivity and low contact resistivity, as shown in this paper. InGaAs quantum-well (QW) MOSFETs with self-aligned Mo and W contacts have exhibited record transconductance and high ON-current [11]–[13].

In spite of these great advances, direct measurements of contact resistance of nanometer-scale refractory contacts to actual nanoscale InGaAs MOSFETs have yet been performed. One reason is that this requires a back-end technology that allows formation of small contacts, something yet to be demonstrated. In this paper, we fabricate and characterize new types of gated and gate-less InGaAs MOSFET arrays with self-aligned W/Mo contacts down to 40 nm in contact length. From these structures, we introduce a characterization method and device model to directly extract the contact resistance of nanometer-scale contacts and dissect all their components. This paper confirms the great promise of this contact scheme, but it also suggests that more research is needed to meet the contact resistance requirements of a future sub-10-nm transistor technology.

This paper is organized as follows. In Section II, we briefly describe the fabrication process and key features of the MOSFET array and gate-less array. In Section III, we show the modeling and analysis of the fabricated array,

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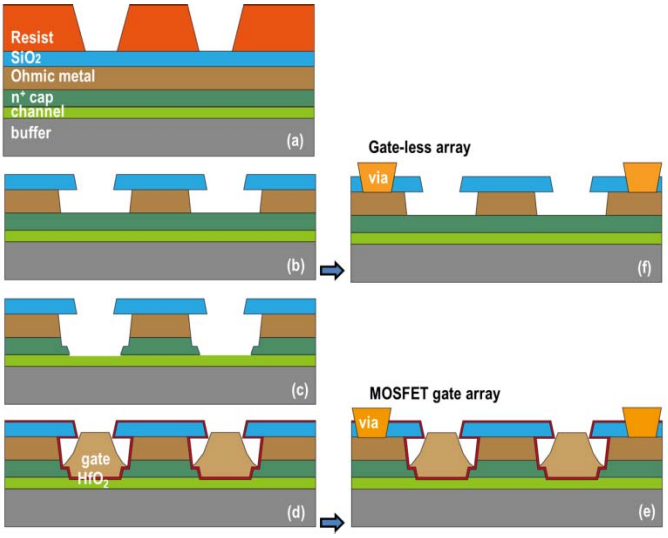

Fig. 1. Schematic of process flow for array fabrication after (a) e-beam lithography, (b) SiO_2 and ohmic metal etching, (c) III–V recess, and (d) gate-stack formation. The finished devices with pads are shown for (e) MOSFET gate array and (f) gate-less array.

particularly the extraction of the contact resistivity of Mo contacts. Section IV discusses the scaling behavior for MOSFET contact resistance. It also includes the benchmarking of the Mo contact in this paper against other contact technologies and the ITRS requirement. Section V states the Conclusion of this paper. This paper is an extension of [13] with further fabrication details and model analysis.

II. Array Design and Fabrication

Two types of array test structures have been used to analyze the electrical characteristics of nanoscale self-aligned ohmic contacts to InGaAs QW MOSFETs. These two arrays and their fabrication procedure are shown in Fig. 1. In essence, a MOSFET array consists of a collection of small footprint MOSFET cells connected in series. A gate-less array is a similar test structure, in which the heavily doped cap has not been recessed and no gate-stacks are deposited.

The device structure and the fabrication procedure for our arrays are similar to that of self-aligned InGaAs MOSFETs described elsewhere [12], [13], [18], [19]. Only a broad outline of the process with previously unpublished relevant details is given here.

The epitaxial structure has been described in [19]. Relevant details are as follows. The cap layer is composed of, from top to bottom, $In_{0.7}Ga_{0.3}As$, $In_{0.53}Ga_{0.47}As$, InP, and InAlAs doped with Si to 3×10^{19} cm^{-3}. The channel consists from top to bottom of an undoped $In_{0.7}Ga_{0.3}As/InAs/In_{0.7}Ga_{0.3}As$ with the layer thicknesses of 3/2/5 nm, respectively. A 3-nm-thick undoped InP spacer is inserted between the channel and the doped cap.

The fabrication process follows a contact-first flow. First, the ohmic contact metal structure is composed of 15 nm of Mo, followed by 15 nm of W, both deposited by high-vacuum sputtering. Under proper deposition conditions [19], the film resistivity, ρ, of Mo is as low as $1.4–1.5 \times 10^{-5}$ $\Omega \cdot$ cm, with a similar value for W. Hence, our 30-nm-thick W/Mo metal stack exhibits a sheet resistance of $R_{sh,m} = 4.6$ $\Omega/\square$.

Second, SiO_2 is deposited, and gate e-beam lithography is performed next using a 120-nm-thick ZEP-520A resist layer. We must ensure that the resist is thick enough to withstand all the subsequent RIE steps, but not too thick to compromise the minimum attainable line spacing [Fig. 1(a)]. This is because a high-aspect-ratio resist pattern can be easily deformed in the subsequent process.

After e-beam lithography, SiO_2, W, and Mo are etched by RIE sequentially. The etching selectively stops at the n^+-InGaAs surface. After eliminating the e-beam resist, the sample is cleaved into two. One piece is reserved to form a gate-less array [Fig. 1(b)], while the rest goes on to become a MOSFET array by fabricating a gate-stack self-aligned to the RIE opening in the ohmic contact structure. This is accomplished by a two-step III–V recess that is carried out through a combination of dry etch and digital etch [Fig. 1(c)]. This approach affords precise channel thickness control as described in detail in [13] and [18]. After this, 2.5-nm Atomic Layer Deposition HfO_2 is deposited as gate insulator, followed by the Mo gate electrode patterning [Fig. 1(d)].

At this point, the two samples are reunited and the process concludes with via opening and pad deposition. Vias and pads are defined only on the long contacts (>10 μm) at the two ends of each array with the inner contacts left floating. Schematics of the finished MOSFET array and gate-less array are shown in Fig. 1(e) and (f), respectively.

Arrays with different gate and contact dimensions and number of cells have been fabricated. The elemental cells of MOSFET array and gate-less arrays are shown in Fig. 2(a). As shown, one cell contains one contact (of length L_c), two half gates (total length L_g), and two access regions (each of length L_{access}). The space occupied by one full cell is its pitch size ($L_p = L_c + L_g + 2L_{\text{access}}$). A zero-cell device becomes a normal MOSFET with long contacts. In this paper, we have fabricated array structures with one to four cells, L_c from 40 to 800 nm and L_g from 40 to 130 nm. L_{access} is fixed at 15 nm. The contact length is estimated from Transmission Electron Microscopy (TEM) images and the respective lithography patterns.

Scanning Electron Microscopy top views of a MOSFET array with three cells are shown in Fig. 2(b) and (c). This is a typical MOSFET layout except that in the gate region there are four gates separated by three inner contacts. All gates are connected to the same gate pad. The inner contacts are left floating. Two outer contacts are connected to SD pads.

Fig. 3(a) shows a cross-sectional TEM of a one-cell MOSFET array with $L_p = 200$ nm, $L_c = 40$ nm, and $L_g = 130$ nm. Fig. 3(b) shows a two-cell MOSFET array with $L_p = 150$ nm, $L_c = 80$ nm, and $L_g = 40$ nm. These are the smallest contact length and pitch sizes in a working InGaAs FET structure demonstrated to date.

III. Cell Resistance Measurements and Analysis

MOSFET array characterization is performed by biasing the gate pad that connects all the gates to V_g. The two outer contacts are connected to the SD pads and biased

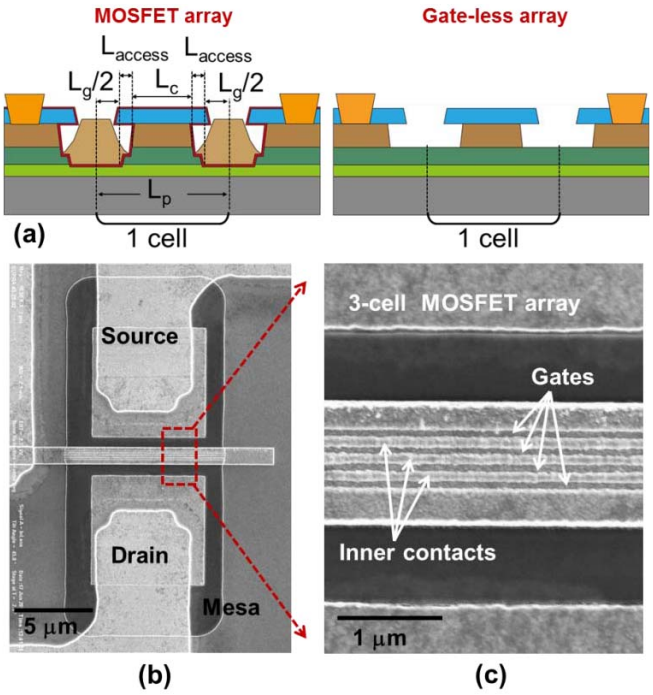

Fig. 2. (a) Schematic of a one-cell MOSFET array (left) and a one-cell gate-less array (right). (b) Top view of a three-cell MOSFET array. (c) Enlarged view showing the gate and contact structure.

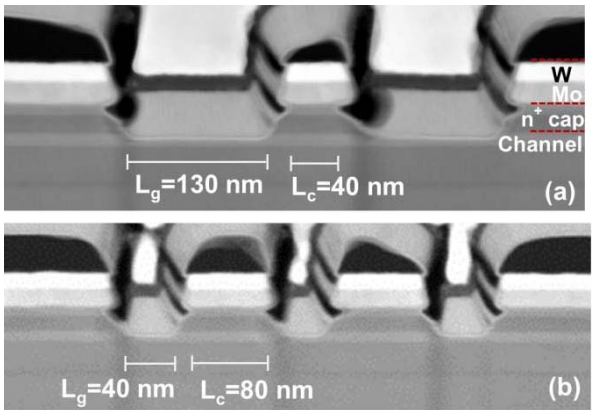

Fig. 3. Cross-sectional TEM of tight-pitch MOSFET arrays with a different contact length, gate length, and pitch size. (a) $L_c = 40$ nm, $L_g = 130$ nm, and $L_p = 200$ nm. (b) $L_c = 80$ nm, $L_g = 40$ nm, and $L_p = 150$ nm. In all cases, $L_{\text{access}} = 15$ nm.

at V_s and V_d, respectively. The inner contacts are floating. Fig. 4(a) shows the transfer characteristics of a MOSFET array with $L_g = 100$ nm, $L_c = 500$ nm, and three cells biased in the linear regime with $V_{\text{ds}} = 50$ mV. Fig. 4(a), in which $V_{\text{gt}} = V_{\text{gs}} - V_t$, also shows the linear characteristics of a zero-cell device which is a normal MOSFET with long contacts. A three-cell long-contact array is equivalent to connecting four identical MOSFETs in series. In the linear regime, the total resistance seen between the two end-contacts is four times that of the zero-cell case. This is consistent with the characteristics of Fig. 4(a).

For high gate overdrive, the I_d–V_{gt} characteristics plateau and the transconductance g_m approach zero. The total

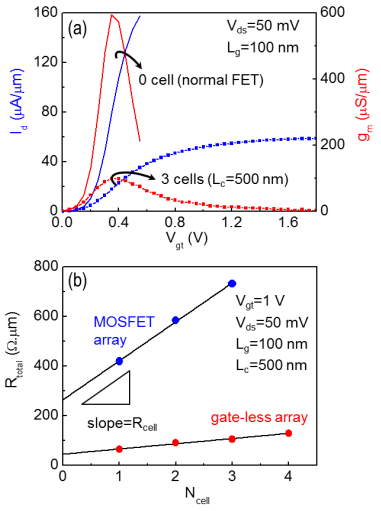

Fig. 4. (a) Linear transfer characteristics of a MOSFET array with three cells, $L_g = 100$ nm and $L_c = 500$ nm as well as a normal transistor with the same L_g. (b) Example of R_{cell} extraction from the slope of total resistance versus number of cells in a gate-less array and a MOSFET array.

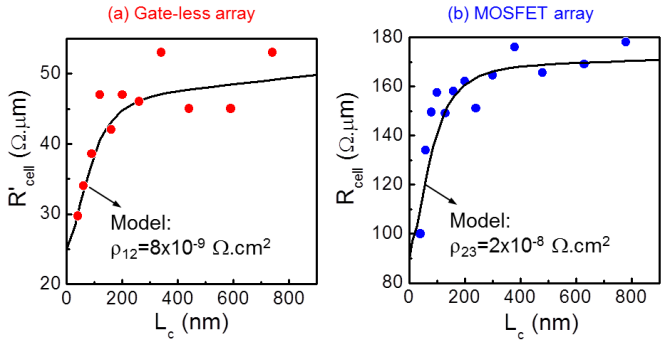

Fig. 5. (a) R'_{cell} versus L_c in gate-less arrays. (b) R_{cell} versus L_c in MOSFET arrays ($L_g = 100$ nm). Solid symbols are for experiment results and line is for a model. The model allows the extraction of ρ_{12} and ρ_{23}, respectively.

resistance of the structure can be extracted as $R_{\text{total}} = V_{\text{ds}}/I_d$. For $V_{\text{gt}} > 0.8$ V, measured R_{total} is rather independent of V_{gt} and is more reliable. In this paper, we have used a value of $V_{\text{gt}} = 1$ V for R_{total} extraction.

Fig. 4(b) shows the measured R_{total} for MOSFET arrays and gate-less arrays with $L_c = 500$ nm as a function of the number of cells, N_{cell}. The MOSFET array has $L_g = 100$ nm. The end-to-end resistance of the MOSFET array cell, R_{cell}, and gate-less array cell, R'_{cell}, can be extracted from the slope of the respective R_{total} versus N_{cell} plots (in blue and red, respectively).

The extracted cell resistance from gate-less arrays and MOSFET arrays with varying contact lengths is shown in Fig. 5(a) and (b), respectively. In gate-less array, R'_{cell} is $\sim 50\ \Omega \cdot \mu$m in the long-contact range and is reduced to $\sim 30\ \Omega \cdot \mu$m when $L_c = 40$ nm. There is a weak dependence of R'_{cell} on L_c for long contacts, but a rapid reduction occurs for $L_c < 200$ nm. A similar trend is observed in the MOSFET array, but the magnitude change of R_{cell} with L_c is larger. The gate length in all these devices is $L_g = 100$ nm.

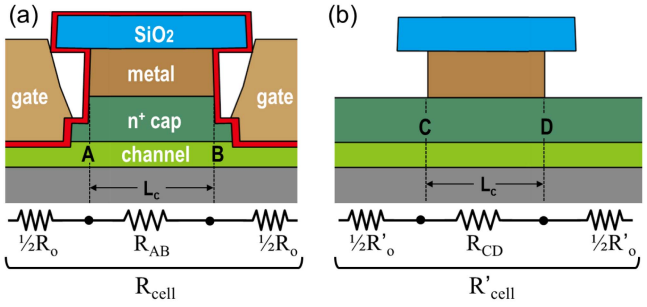

Fig. 6. Schematic cross section of one cell for (a) MOSFET array and the circuit model for R_{cell} and (b) gate-less array and the circuit model R'_{cell} (see text).

The characteristic shape of the evolution of R_{cell} and R'_{cell} with L_c has a common origin. Referring to the MOSFET array, this shape arises from the shunting effect of the contact on the current flow along the channel in an elemental cell. For short contacts, the current path remains mainly in the channel and R_{cell} increases with L_c with a slope that reflects the sheet resistance of the channel under the contact. For long contacts, the current path flows through the contact interface into the metal and back down again at the other end. As a result, the slope of R_{cell} with L_c now reflects the sheet resistance of the contact metal bilayer. The corner value of L_c at which the character of R_{cell} changes is, therefore, twice the transfer length of the contact. Similar arguments apply for the gate-less array.

For a rigorous analysis of R_{cell} and R'_{cell}, we have developed equivalent circuit models, as shown in Fig. 6. In the MOSFET array under the low current condition selected here, the intrinsic channel region behaves as a resistor. In addition, the resistance associated with the access region is also constant. The sum of these resistances is denoted by R_o in Fig. 6(a). The difference between R_{cell} and R_o, that is, the resistance seen between A and B in Fig. 6(a), R_{AB}, depends on the contact length, L_c, of the cell. A and B are the projections of the contact edges to the channel. A similar picture applies for the gate-less array [Fig. 6(b)]. In this case, the access resistance component associated with current flow through the cap constitutes a constant offset R'_o. The resistance in the contact region is now between C and D, R_{CD}, where C and D are the projections of the contact edges to the cap. We can then see that in Fig. 5, the $L_c = 0$ extrapolation of the data corresponds to R_o and R'_o, which is 90 and 25 $\Omega \cdot \mu$m, respectively. This includes the sum of the two access resistances to the intrinsic device which does not change as L_c changes. When these values are, respectively, subtracted from R_{cell} and R'_{cell}, the remaining portions are the resistances R_{AB} and R_{CD}.

For further analysis of R_{AB} and R_{CD}, we now focus on the contact region with a cross-sectional schematic shown in Fig. 7(a). It consists of a stack of three layers: 1) ohmic metal characterized by a sheet resistance $R_{\text{sh},m}$; 2) n^+ cap characterized by $R_{\text{sh},n}$; and 3) channel characterized by $R_{\text{sh},c}$. The interface between these three layers is characterized by two contact resistivities: 1) ρ_{12} between metal and cap and 2) ρ_{23} between cap and 2DEG channel. This multilayer system can then be modeled as a distributed resistor network,

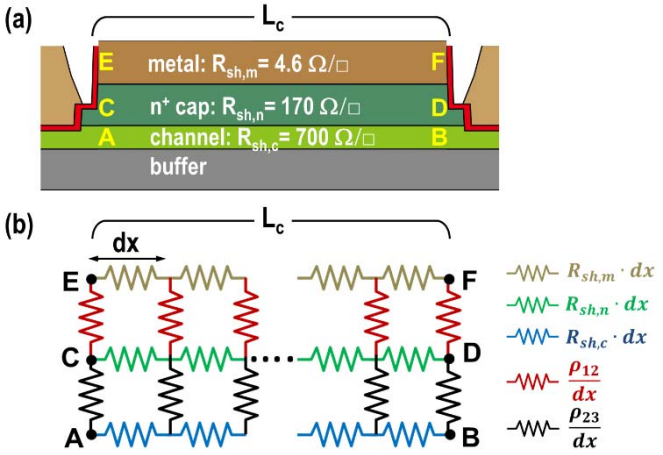

Fig. 7. (a) Schematic of contact structure containing three parallel conducting layers. (b) Distributed equivalent circuit model for contact layer structure.

as shown in Fig. 7(b). If we define an elemental length dx, the lateral resistors in each layer have a value $R_{\text{sh}} \cdot dx$ and the vertical resistors connecting them are ρ_{xy}/dx, all in units of $\Omega \cdot \mu$m.

A netlist for this resistive network was generated in the MATLAB and solved using the HSPICE. We have used $dx = 10$ nm, a value small enough to model the smallest contacts ($L_c = 40$ nm).

This model allows the contact resistivities, ρ_{xy}, to be extracted once the sheet resistances of the individual conducting layers R_{sh} are provided as inputs. These are obtained from independent measurements on devices and test structures located elsewhere on the same chip. The sheet resistance of the channel, $R_{\text{sh},c}$, is obtained from the measurements of ON-resistance on transistors with different values of L_g. As in the MOSFET array, R_{ON} is measured at a gate overdrive that results in the transistor g_m approaching zero. The sheet resistance of the n^+ cap, $R_{\text{sh},n}$, and the metal, $R_{\text{sh},m}$, is obtained from TLM measurements. $R_{\text{sh},n}$ is confirmed with Hall measurements. The values of all these parameters are given in Fig. 7(a).

With these values as inputs, ρ_{12} is extracted by optimizing the model fitting against the experimental results in Fig. 5(a). Given ρ_{12}, ρ_{23} can be extracted from the optimization of the model against the data in Fig. 5(b). The resulting model (continuous lines) reproduces the experimental measurements rather well. The value of the contact resistivity between Mo and n^+ cap that emerges is $\rho_{12} = (8 \pm 2) \times 10^{-9}\ \Omega \cdot \text{cm}^2$. This is consistent with the value obtained from nano-TLM structures with nanoscale Mo contacts [15]. The contact resistivity between the n^+ cap and the 2DEG channel that is obtained is $\rho_{23} = (2 \pm 0.8) \times 10^{-8}\ \Omega \cdot \text{cm}^2$. This is a significant component of the overall contact resistance that has never been isolated before.

The distributed electrical model that we have developed for our contacts provides insightful information on their electrical behavior. The current through each resistance element can be read out of the HSPICE simulations. We use $i_{//}$ to denote the normalized current in the lateral direction, and $i_{\perp}$ for

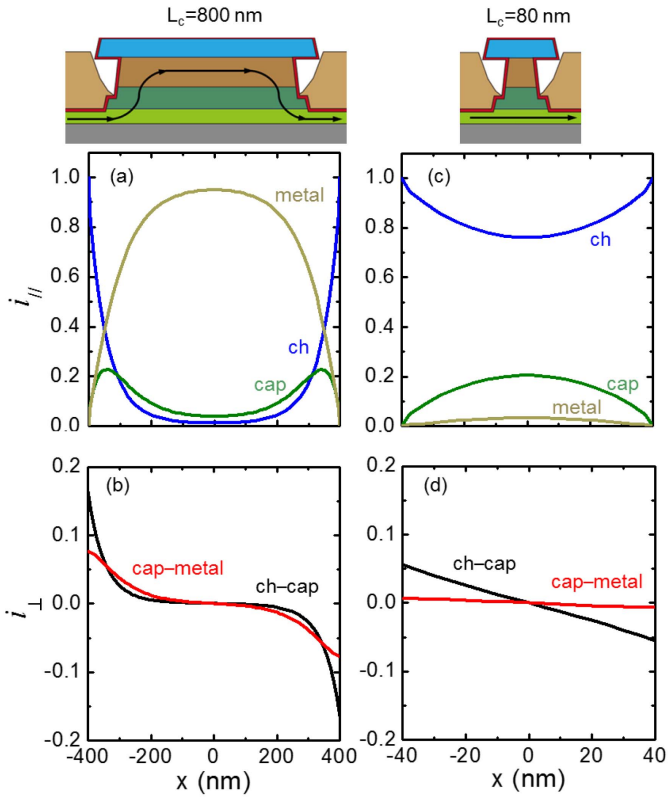

Fig. 8. Model of (a) and (c) lateral current and (b) and (d) vertical current flow in a long contact with $L_c = 800$ nm and a short contact with $L_c = 80$ nm, respectively. Currents in the different layers are normalized to the total terminal current. Positive sign of $i_\perp$ represents upward current flow and vice versa. Top: dominant current path in long and short contacts, respectively.

the vertical direction. The currents are normalized to the magnitude of the total terminal current flowing into the device at the two ends. Hence there are three components of $i_{//}$ for each of the layers in the stack that at a particular location x add up to 1.

Fig. 8 shows $i_{//}$ and $i_\perp$ in a MOSFET contact as a function of lateral location (x) for two contact lengths, 800 and 80 nm. In both cases, $i_{//,c}$ is 1 at the edge, since this is how the current is fed into the structure. In the long contact, $L_c = 800$ nm [Fig. 8(a)], $i_{//,c}$ gradually reduces from the edge toward the center of the contact. In the limit of very long contact, $i_{//}$ should follow the current divider relationship:

$$i_{//,m} : i_{//,n} : i_{//,c} = R_{\mathrm{sh},m}^{-1} : R_{\mathrm{sh},n}^{-1} : R_{\mathrm{sh},c}^{-1}.$$

Indeed, we see that for $L_c = 800$ nm, the ohmic metal conducts over 90% of the total current in the middle of the contact [Fig. 8(a)]. In this regime of L_c, R_{cell} versus L_c should have a slope that approaches $R_{\mathrm{sh},m}$. This is in good agreement with the data in Fig. 5(b), where we see $dR_{\mathrm{cell}}/dL_c = 5\ \Omega/\square$ in the long-contact regime.

Fig. 8(b) shows the vertical currents through the long contact. It flows across the vertical resistors to reach the ohmic/cap layers in the leading edge and leaves the ohmic/cap layers in a symmetric manner at the other end. In the middle, $i_\perp$ is zero.

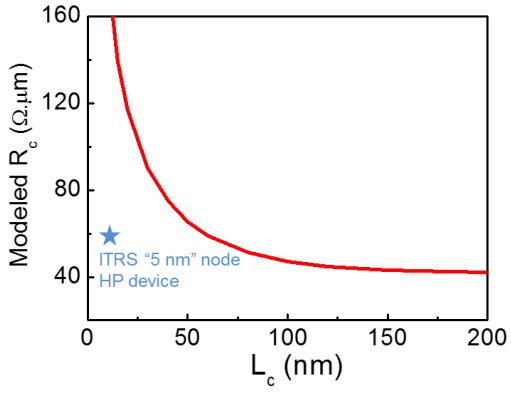

Fig. 9. Modeled contact resistance versus contact length for the contact scheme investigated in this paper. This is the estimated resistance between nodes A and E in Fig. 7.

Fig. 8(c) and (d), respectively, shows $i_{//}$ and $i_\perp$ for a short contact ($L_c = 80$ nm). The current mostly stays in the channel, because it presents the smallest resistive path (top right schematic in Fig. 8). Hence, in this region, the slope of R_{cell} versus L_c in Fig. 5(b) follows $R_{\mathrm{sh},c}$. This is similar to Fig. 5(a). In the fitting curves of Fig. 5(a) and (b), the slope at small L_c is 190 and 560 $\Omega \cdot \mu$m, respectively, and is in reasonable agreement with $R_{\mathrm{sh},n}$ and $R_{\mathrm{sh},c}$, respectively.

It should be noted that the MOSFET model used in this analysis assumes standard diffusive transport through the channel, which leads to $R_{\mathrm{ch}} = 0$ for $L_g = 0$. However, it has been shown that for very short Si MOSFETs operating in the quasi-ballistic regime, R_{ch} approaches the ballistic resistance which is also referred to as the ballistic contact resistance [20]. In III–V devices with lower effective mass than in Si quasi-ballistic operation can extend to higher L_g values comparable with those used in this paper. If so, then the contact resistance between channel and n^+ cap may be somewhat overestimated. A more advanced device model, including ballistic effects, is required to account for this, which is outside the scope of this paper.

IV. Projections for MOSFET Contact Resistance and Benchmarking

The characterization and the analysis of the contact scheme that is presented in this paper enable us to model the contact resistance expected in actual scaled MOSFETs. We can do this by extracting the equivalent resistance between nodes A and E in Fig. 7. Note that this is the resistance from the metal layer to the edge of the channel and not just to the edge of the cap, as extracted in a TLM measurement. The result is shown in Fig. 9 as a function of contact length. The star sign in Fig. 9 indicates the ITRS required dimension and R_c for the 5-nm node HP device [3].

The estimation in Fig. 9 reveals that the long contacts should have a contact resistance of 40 $\Omega \cdot \mu$m (one side). For shorter contacts, R_c shoots up as L_c becomes smaller than the transfer length which we estimate at ~110 nm. At L_c of 10 nm, the contact resistance is estimated to be 260 $\Omega \cdot \mu$m. As the ITRS goal is 60 $\Omega \cdot \mu$m at $L_c = 10$ nm [3], we conclude that the significant improvements are still required.

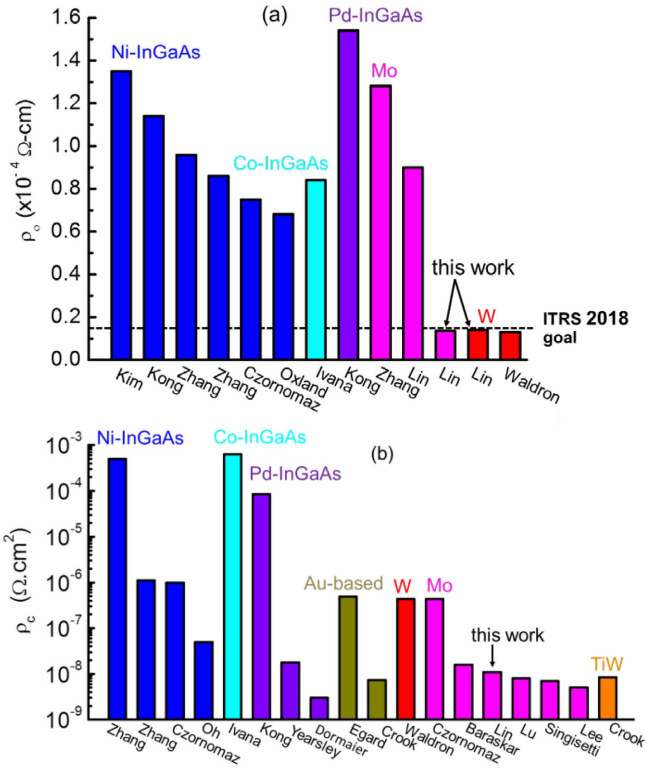

Fig. 10. Benchmarking of (a) film resistivity ρ_o of contact metals [9], [14], [17], [18], [21]–[28] and (b) contact resistivity ρ_c [13]–[16], [22]–[25], [27]–[33], for different contact technologies for n-type InGaAs MOSFETs.

The contact technology studied in this paper has been benchmarked in Fig. 10 against other contact technologies recently published for n-type InGaAs MOSFETs or n^+ InGaAs. The comparison includes refractory metals, non-Au-based InGaAs metal alloys, and Au-based contacts. Two properties of the contact metal are graphed: (a) the metal film resistivity, ρ_o and (b) the contact resistivity, ρ_c.

The film resistivity is defined as the product of sheet resistance of the metal or metal alloy and its thickness, $\rho_o = R_{\rm sh} \cdot t$. ITRS specifies the requirement for the sheet resistance and thickness of future silicides [3]. In essence, this is equivalent to the resistivity of the ohmic metal film. The film resistivity ρ is shown in Fig. 10(a). For comparison, the 2018 ITRS requirement is also specified as $\rho_o = 1.6 \times 10^{-5}\ \Omega \cdot$ cm, equal to that of nickel silicide [3]. The graph reveals that most of the ohmic metals or metal alloys used in InGaAs MOSFETs to date have resistivities much higher than the required value. Typical film resistivity of the popular Ni–InGaAs, Co–InGaAs, and Pd–InGaAs alloys is between 7×10^{-5} and $1.5 \times 10^{-4}\ \Omega \cdot$cm, about 5 to 10 times the ITRS requirement. In contrast, the refractory metals used in this paper exhibit film resistivity that satisfies the ITRS requirement. In accomplishing this, the deposition method plays an important role [18], [34]. The high-resistivity Mo films in Fig. 8(a) are deposited by evaporation [17]. Sputtering yields low-resistivity Mo and W films.

Fig. 10(b) shows the reported contact resistivity values on n^+ InGaAs. InGaAs alloys and Au-based contacts on n-type InGaAs yield results that vary dramatically from 5×10^{-9} to $6 \times 10^{-3}\ \Omega \cdot$ cm^2. The lowest contact resistivity of $4 \times 10^{-9}\ \Omega \cdot$ cm is reported for Pd–InGaAs [30], and $5 \times 10^{-9}\ \Omega \cdot$ cm for Au-based contacts [29]. A contact resistivity of $\rho_c = 8 \times 10^{-9}\ \Omega \cdot$ cm^2 has been obtained in this paper using Mo/W (Mo at the interface with the semiconductor). This value is consistent with earlier reports for Mo contacts on n^+ InGaAs [15], [16], [33]. All those demonstrations have utilized techniques to preserve the pristine surface of the n^+ InGaAs before Mo deposition, for example, the metal-first process in this paper and [15], an oxidizer/acid treatment (digital etch) for Fin smoothing [16], and *in situ* Mo deposition [33]. The extremely low contact resistivity is an attractive property of Mo-based contacts. The Landauer limit of any metal contact to n^+ InGaAs is estimated to be $\sim 1 \times 10^{-9}\ \Omega \cdot$ cm^2 [35]. This suggests that there is still room for the reduction of contact resistivity between Mo and n^+ cap.

V. Conclusion

We have fabricated the InGaAs MOSFET arrays and gateless arrays with a very tight pitch. Our self-aligned process enables the fabrication of MOSFET unit cells with 40-nm contact size and 150-nm pitch size. We have used these arrays to characterize the electrical properties of nanometer-scale Mo/W ohmic contacts. An HSPICE model has allowed us to extract a contact resistivity of $8 \times 10^{-9}\ \Omega \cdot$ cm^2 between Mo and n^+ InGaAs, and a contact resistivity of $2 \times 10^{-8}\ \Omega \cdot$ cm^2 between n^+ InGaAs and the 2DEG channel. A benchmarking study with other contact technologies on n-type InGaAs shows two advantages of a refractory contact scheme. It has the lowest film resistivity of all reported contact schemes, and it yields among the lowest contact resistivities.

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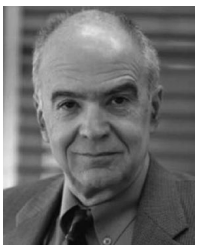

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